FUDAN MICROELECTRONICS

复旦微电子

FM11RF005U
512Bits EEPROM Contactless Smart Card IC

Functional Specification

May. 2008

Content

1. Features

- **Contactless Communications RF Interface**
  - Contactless transmission of data and supply (no battery needed)
  - Operating distance: up to 100mm (depending on antenna geometry)
  - Operating frequency: 13.56MHz
  - Fast communication baud rate: 106Kbit/s
  - Half duplex communication protocol using handshake
  - Modulation and encoding comply with ISO/IEC 14443 Type-A protocol
  - Answer to request: comply with ISO/IEC14443 Type-A protocol.
  - Typical transaction time: ≤ 35ms
  - True anti-collision
- **EEPROM**
  - 512 bits EEPROM memory.
  - Organized in 16 blocks of 4 bytes each
  - 32 bit User definable One Time Programmable (OTP) area
  - 384 bit user r/w area (12 pages).
- **High Security**
  - 7 bytes serial number (cascade level2 according to ISO/IEC 14443-3
  - Field programmable read-only locking function per page
- **High Reliability**
  - Endurance: 100,000cycle
  - Data Retention: 10 Years

2. Product Overview

2.1. Instruction

The FM11RF005U is the contactless smart card IC according to ISO14443 Type-A developed by Shanghai FM Co., LTD. This device has 512 bits EEPROM organization. The maximum communication range between the reader antenna and contactless card is approximately 10cm. Data is exchanged half duplex at a 106-kbit/s rate.

Depending on the field programmable read-only locking and One Time Programmable (OTP) function, the FM11RF005U provides advanced security level and logical transaction function. As a style of multi-application card, the FM11RF005U is wildly used in the low-cost field of city public transport、variously charging payment card、data acquisition systems and comparable application.

The Contactless smart card contains three components: FM11RF005U chip、antenna and the card base with PVC (or PET) material. No battery is needed. When the chip is positioned in proximity of the coupling device antenna, the high speed RF communication interface allows to transmit data with 106 Kbit/s.

2.2. Block Diagram

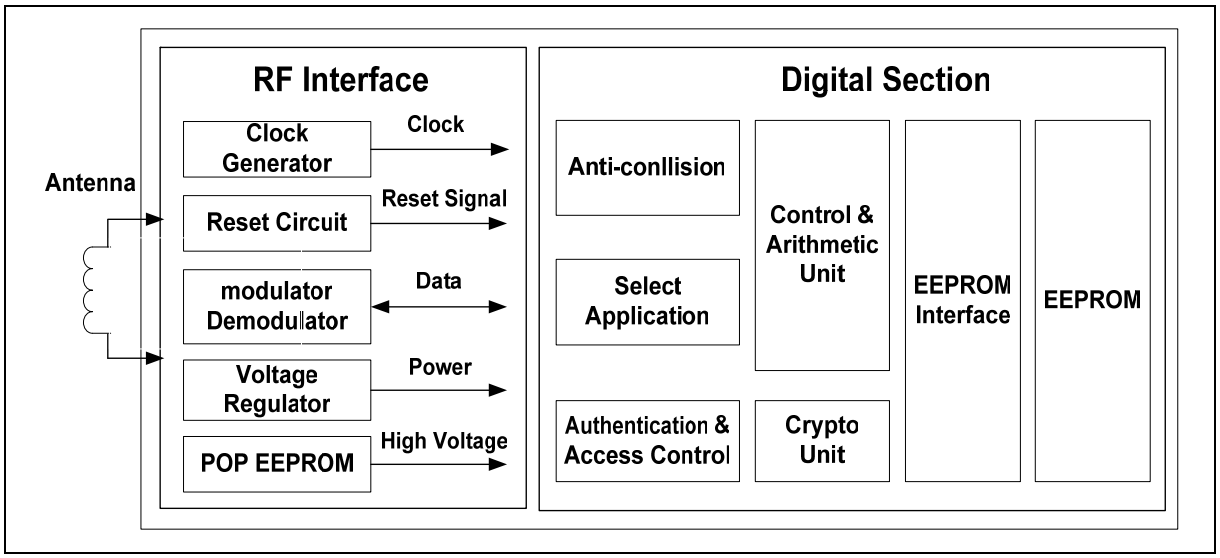


Figure 2-1 FM11RF005U Block Diagram

3. Command Set

3.1. Command Description

REQALL/REQA: establishes the communication between card and RWD, the REQALL/REQA command has to be passed before implementing the further commands. The difference of REQA and WUPA is the REQA will only response on the idle state, thus WUPA will response at two state of idle and halt.

ANTICOLLISION/SELECT: double command: Cascade Level 1 and Cascade Level 2, respectively return the first 3 bytes and the second 4 bytes of UID.

Read: read out seriate 4 pages (16 bytes) from specified address.

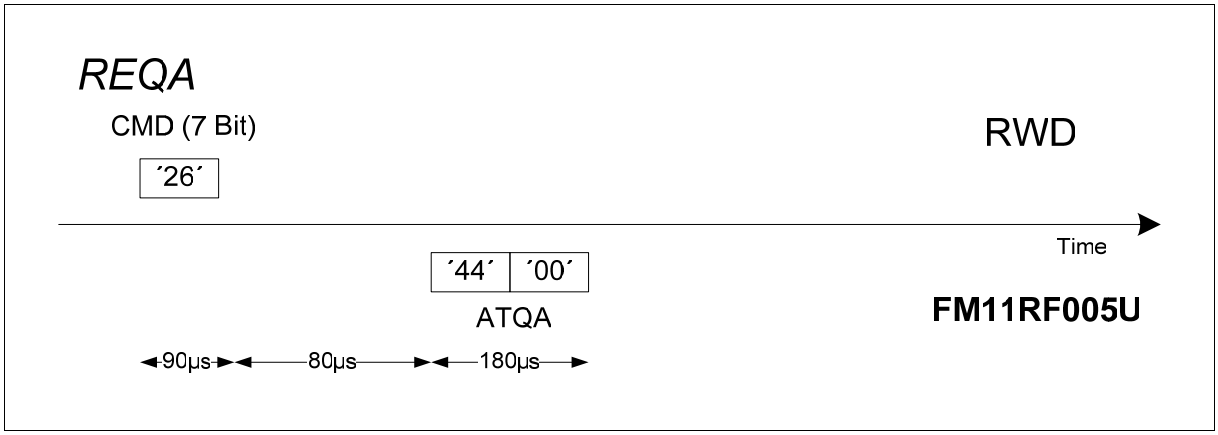
Halt: make the card return to the halt state from the active state.

Write: write and the compatibility write CMD. The write command write data to one page and finished at once, however, the compatibility write CMD also write one page but it transmit 16 bytes data at twice, first send the compatibility write command and address to card, after acknowledges it is right the card will answer a response, and then transmit the data waiting to be written.

3.2. Command Format

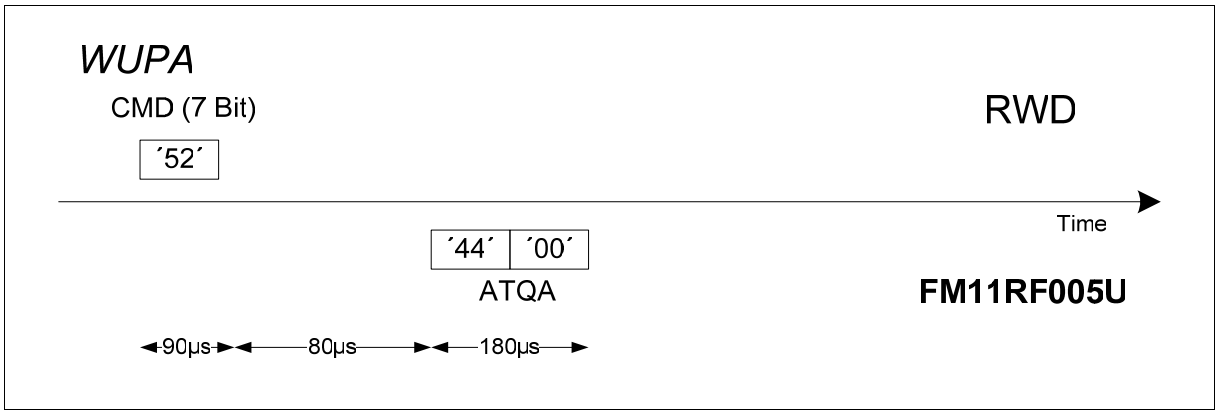
1、REQA

Code	Parameter	Data	Integrity mechanism	Response
0x26（7Bit）	-	-	-	0x0044



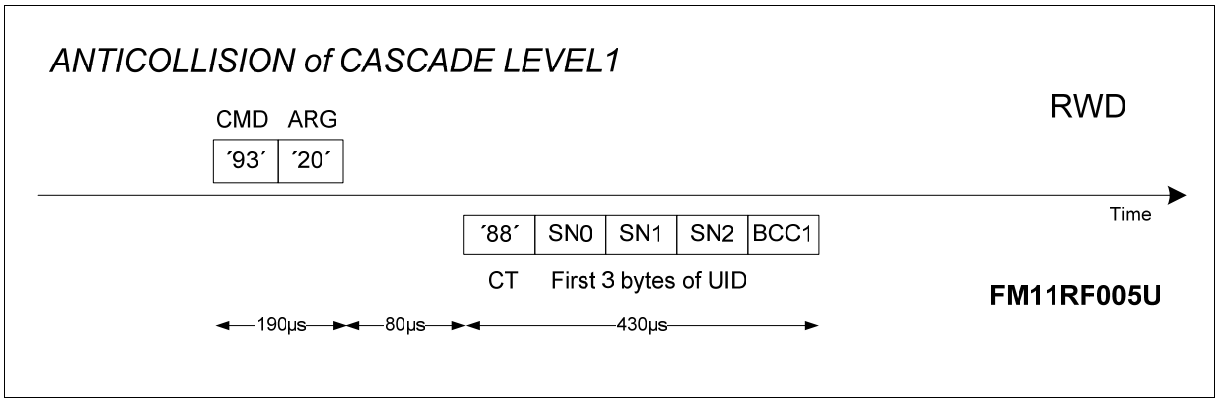
2、WUPA

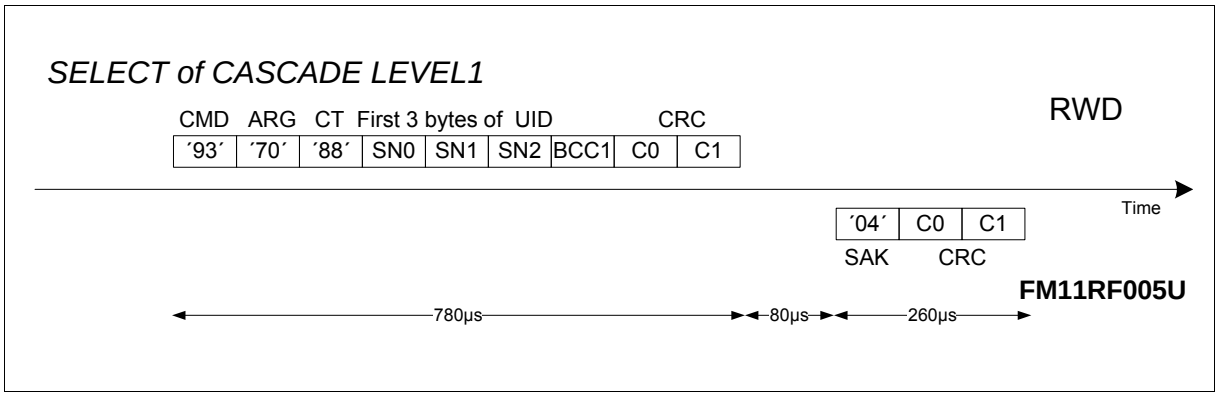
Code	Parameter	Data	Integrity mechanism	Response
0x52（7Bit）	-	-	-	0x0044



3、ANTICOLLISION AND SELECT OF CASCADE LEVEL 1

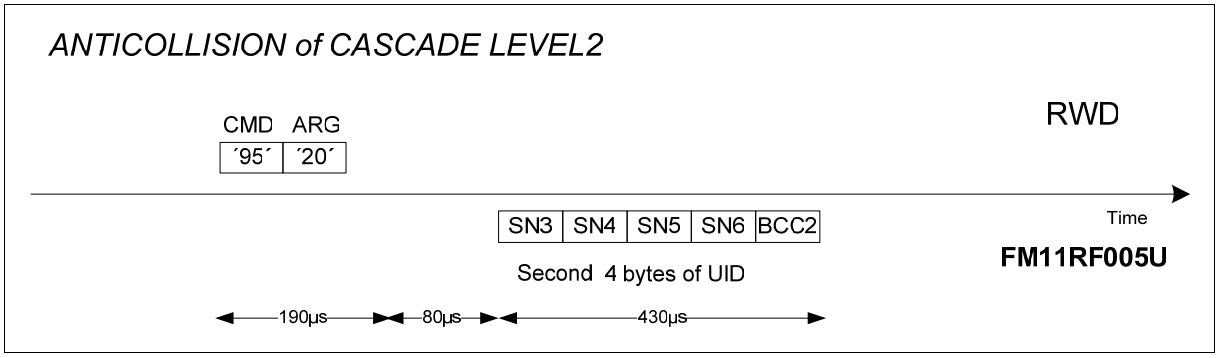
Code	Parameter	Data	Integrity mechanism	Response
Anticollision: 0x93	0x20 - 0x67	Part of UID	Parity	Rest of UID
Select: 0x93	0x70	First 3 bytes of UID	Parity、BCC、CRC	SAK（’04’）

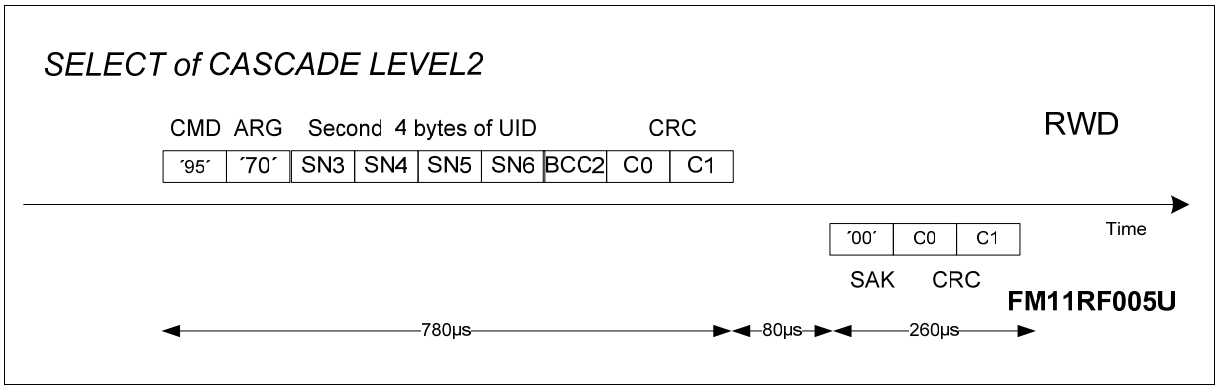




4、ANTICOLLISION AND SELECT OF CASCADE LEVEL 2

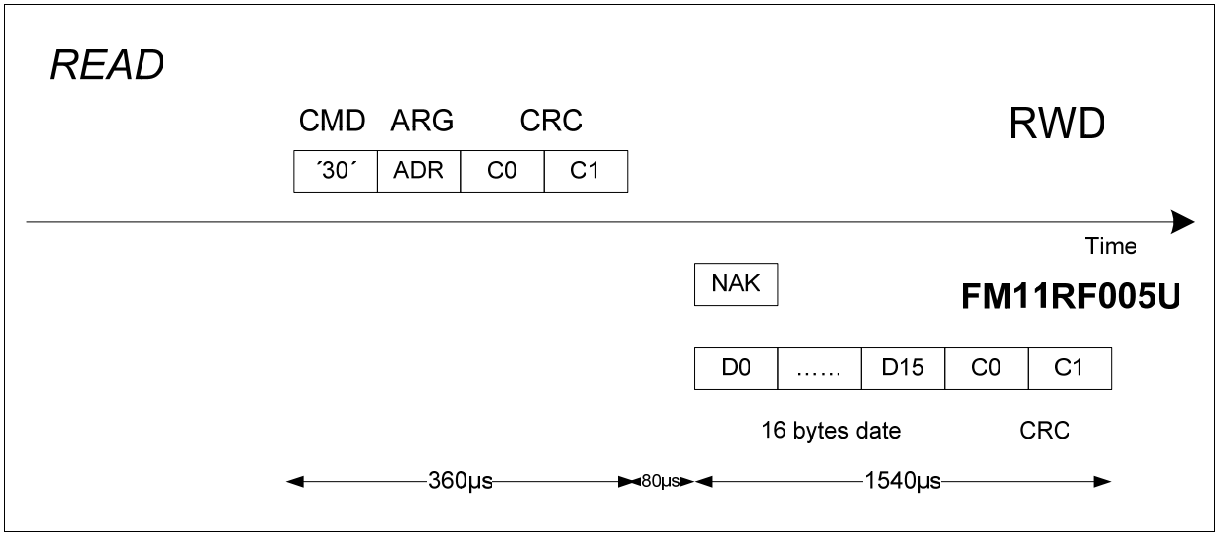
Code	Parameter	Data	Integrity mechanism	Response
Anticollision: 0x95	0x20 - 0x67	Part of UID	Parity	Rest of UID
Select: 0x95	0x70	Second 4 bytes of UID	Parity、BCC、CRC	SAK（'00'）





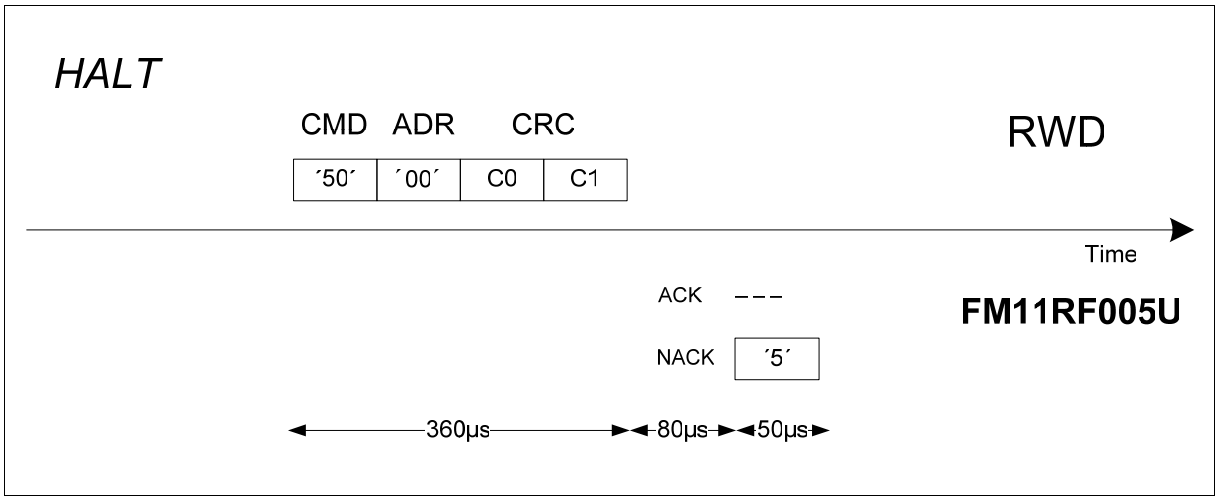
5、READ

Code	Parameter	Data	Integrity mechanism	Response
0x30	ADR（8Bit）	-	CRC	16 Byte Date



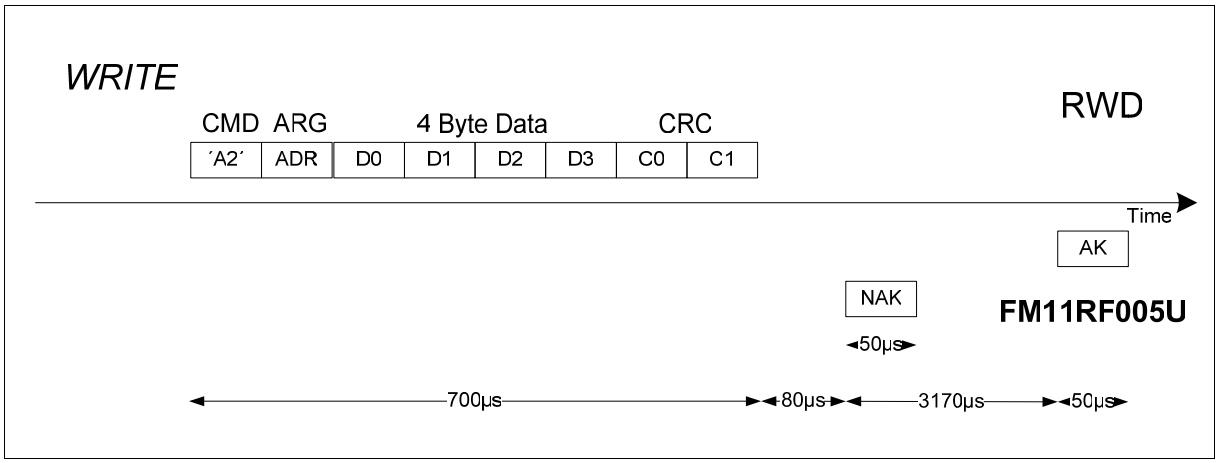
6、HALT

Code	Parameter	Data	Integrity mechanism	Response
0x50	0x00	-	Parity、CRC	NAK、AK



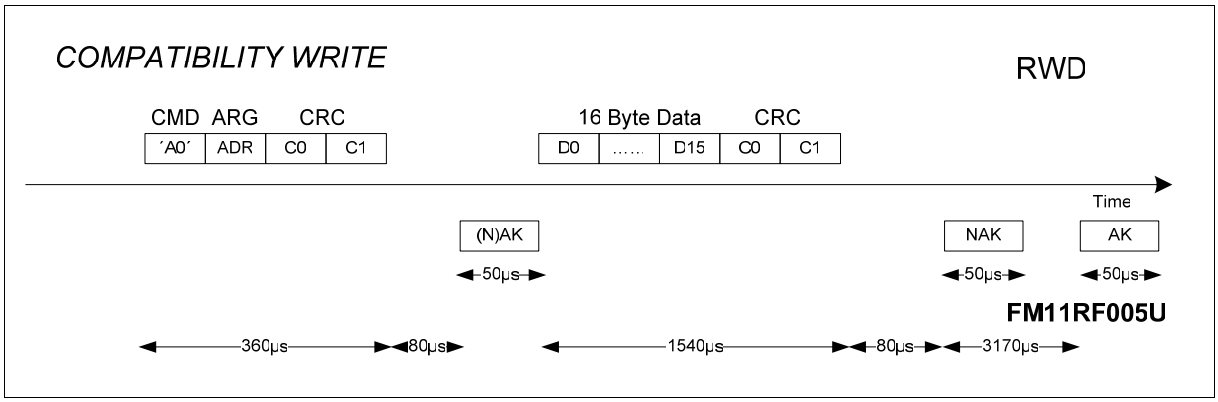
7、WRITE

Code	Parameter	Data	Integrity mechanism	Response
0xA2	ADR（8Bit）	4 Byte	Parity、CRC	NAK、AK



8、COMPATIBILITY WRITE

Code	Parameter	Data	Integrity mechanism	Response
0xA0	ADR（8Bit）	16 Byte Data	Parity、CRC	NAK or AK



Note:

1. All of upwards commands are accommodated from RWD to card.
2. The CASCADE LEVEL1 will be implemented only at the Ready1state; CASCADE LEVEL2 will be implemented only at the Ready2 state.
3. Even though 16 bytes are transferred to the FM11RF005U, only the least significant 4 bytes will be written to the specified address.
4. During the communication there is a Parity bit after each byte, but parity bit don't need implement the CRC.

4. State Diagram

The commands are initiated by the RWD and controlled by the command interpreter of the FM11RF005U. It handles the internal states and generates the appropriate responses.

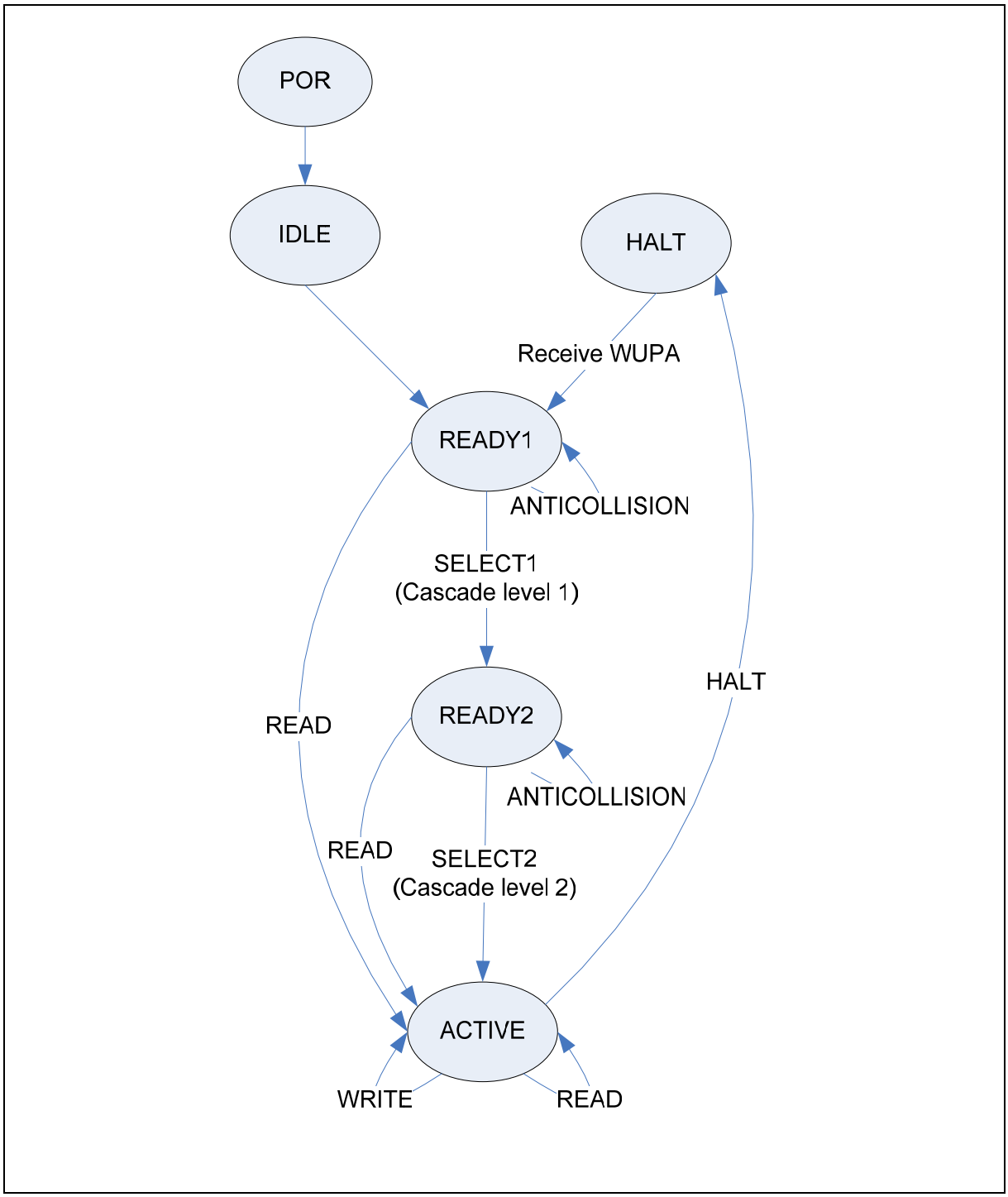


Figure 4-1 FM11RF005U Card State Conversion

5. Memory Organization

The 512 bit EEPROM memory of the FM11RF005U is organized in 16 pages with 4 bytes each, one block consists of 16 bytes each.

Byte Number	0	1	2	3	Page No.
Serial Number	SN0	SN1	SN2	BCC1	0
Serial Number	SN3	SN4	SN5	SN6	1
Internal/Lock	BCC2	Internal	Lock0	Lock1	2
OTP	OTP0	OTP1	OTP2	OTP3	3
Data read/write	DATE0	DATE1	DATE2	DATE3	4
Data read/write	DATE4	DATE5	DATE6	DATE7	5
Data read/write	DATE8	DATE9	DATE10	DATE11	6
Data read/write	DATE12	DATE13	DATE14	DATE15	7
Data read/write	DATE16	DATE17	DATE18	DATE19	8
Data read/write	DATE20	DATE21	DATE22	DATE23	9
Data read/write	DATE24	DATE25	DATE26	DATE27	10
Data read/write	DATE28	DATE29	DATE30	DATE31	11
Data read/write	DATE32	DATE33	DATE34	DATE35	12
Data read/write	DATE36	DATE37	DATE38	DATE39	13
Data read/write	DATE40	DATE41	DATE42	DATE43	14
Data read/write	DATE44	DATE45	DATE46	DATE47	15

Table 5-1 FM11RF005U Memory Organization

Note: the page0, page1 and the first byte of page2 are write-protected after having been programmed by the IC manufacturer after production, user can't change those. Other area is user area.。

5.1. UID/Serial Number

The first 2 bytes of Page0、Page1 and Page 2 are serial number:

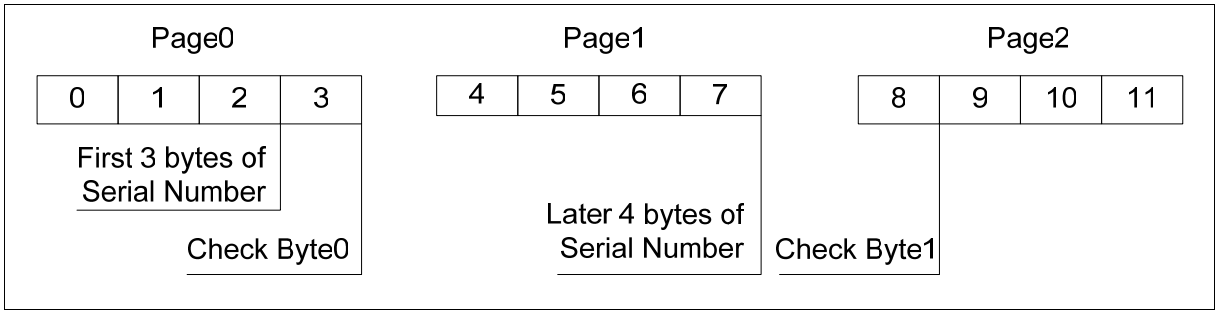


Figure 5-1 FM11RF005U Serial Number

Note: 1、UID is write-protected by the IC manufacture，User can't change it；

2、BCC0=CT ⊕ SN0 ⊕ SN1 ⊕ SN2； BCC1=SN3 ⊕ SN4 ⊕ SN5 ⊕ SN6。

5.2. OTP

Page 3 is the OTP page. It is pre-set to all “0” after production. These bytes may be bit-wise modified by a write command. But this process is irreversibility. Once a bit is set to “1”，it can’t be changed back “0” again.。

5.3. Lock Bytes

The bits of Byte 2 and 3 of page 2 represent the field-programmable read-only locking mechanism.

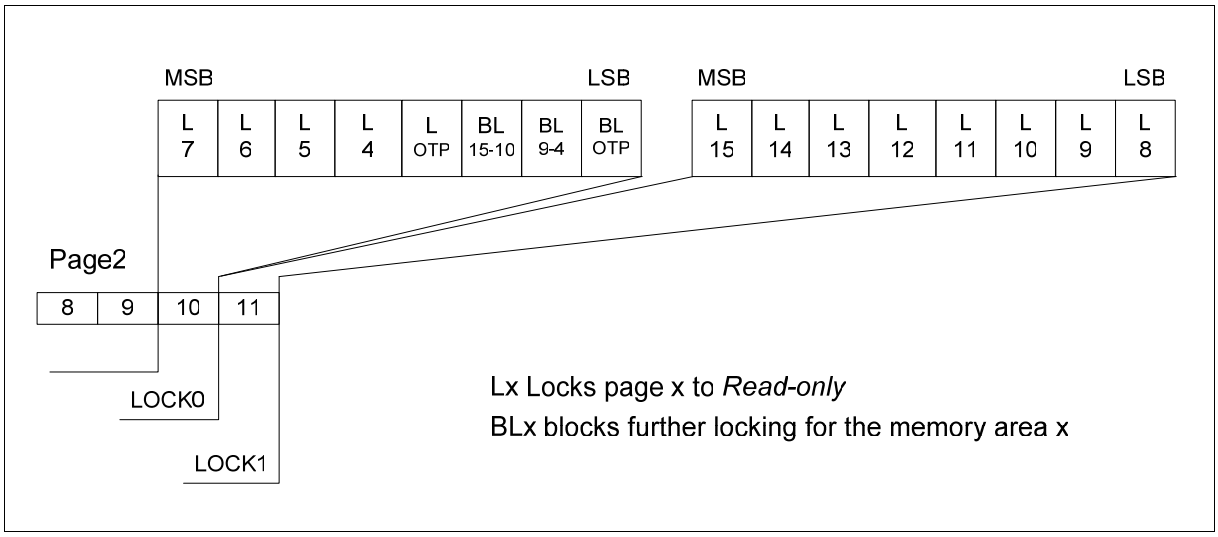


Figure 5-2 FM11RF005U Lock Bytes

Note:

1. After some bits were locked, the rearward write operation on the block-locking bits has no effect until the lock is unlocked.
2. If the bit Lx is set to read-only, the corresponding setting of the BLx will be ignored.
3. If a bit is set to “1”, it can’t be changed back to “0” again.
4. The Locking and block-locking bits can be set via a write command; this process cann’t change the contents of bytes0 and bytes1 of page2.
5. To activate the new locking configuration after a write to the lock bit area, a REQA or WUPA command has to be carried out.

5.4. Data Pages

Page4 to 15 constitute the user read/write area. After production the data pages are initialized to all "0".

Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	Oct. 2007	15		Initial Release.
1.1	May.2008	15	Sales and service	Updated the address of HK office.

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